

FISH & RICHARDSON P.C.

4225 Executive Square
Suite 1400
La Jolla, California
92037

Telephone
619 678-5070

Facsimile
619 678-5099

October 28, 1997

Attorney Docket No.: 07977/192001

Assistant Commissioner for Patents
Washington, DC 20231

Presented for filing is a new original patent application of:

Applicant: HISASHI OHTANI AND ETSUKO FUJIMOTO
Title: SEMICONDUCTOR DEVICE AND METHOD OF
FABRICATING THE SAME

Enclosed are the following papers, including all those required for a filing date under
37 CFR §1.53(b):

Pages of Specification	22
Pages of Claims	4
Pages of Abstract	1
Pages of Declaration	2
Sheets of Drawing	7

Under 35 USC §119, this application claims the benefit of a foreign priority
application filed in Japan, serial number 8-307443, filed October 31, 1996. A certified
copy of the priority application is enclosed.

"EXPRESS MAIL" Mailing Label Number E m 3 6 7 7 6 0 7 8 3 4

Date of Deposit 10 28 97

I hereby certify under 37 CFR 1.10 that this correspondence is being
deposited with the United States Postal Service as "Express Mail Post
Office To Addressee" with sufficient postage on the date indicated
above and is addressed to the Assistant Commissioner for Patents,
Washington, D.C. 20231.

Jennifer H. Payne
Jennifer H. Payne



Frederick P. Fish
1855-1930

W.K. Richardson
1859-1951

BOSTON

HOUSTON

NEW YORK

SOUTHERN CALIFORNIA

SILICON VALLEY

TWIN CITIES

WASHINGTON, DC

FISH & RICHARDSON P.C.

BOX PATENT APPLICATION

October 28, 1997

Page 2


Basic filing fee	\$ 790.00
Total claims in excess of 20 times \$22.00	0.00
Independent claims in excess of 3 times \$82.00	0.00
Multiple dependent claims	0.00
Total filing fee:	\$ 790.00

A check for the filing fee is enclosed. Please charge any other required fees, or apply any credits, to Deposit Account No. 06-1050, referencing the Attorney Docket number shown above.

If this application is found to be INCOMPLETE, or if it appears that a telephone conference would helpfully advance prosecution, please telephone the undersigned at 619/678-5070.

Kindly acknowledge receipt of this application by returning the enclosed postcard.

Respectfully submitted,



Scott C. Harris
Reg. No. 32,030

Enclosures
44242

APPLICATION
FOR
UNITED STATES LETTERS PATENT

TITLE: SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING
THE SAME

APPLICANT: HIDSDDHI OHTANI AND ETSUKO FUJIMOTO

"EXPRESS MAIL" Mailing Label Number Em367766783US

Date of Deposit 10-28-97

I hereby certify under 37 CFR 1.10 that this correspondence is being deposited with the United States Postal Service as "Express Mail Post Office To Addressee" with sufficient postage on the date indicated above and is addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231.

Jennifer H. Payne
Jennifer H. Payne

known that the method of using an interlayer dielectric film of silicon nitride for TFTs is advantageous, as described in Japanese Patent Unexamined Publication No. 326768/1995. With this method, if the etch rates of silicon nitride and the active layer are not sufficiently high where the interlayer dielectric is etched, it is difficult to detect the end point of the etching, since the silicon nitride layer is approximately 10 times as thick as the active layer.

Other problems may arise, depending on circuits. For example, in the structure shown in Figs. 2(A)-2(F), the drain 27 or silicide 31 must gain access to the gate interconnect 25 via the top layer of interconnect metal 35, i.e., via two contacts. Contacts tend to produce many defects and have large resistivities. Obviously, the number of the contacts included in the circuit should be reduced to a minimum. Furthermore, the silicide layer is very thin, producing many defects at the contacts, though the possibility of overetching decreases. Consequently, the contact holes are required to have sufficient spread, which is an obstacle in achieving higher circuit density.

SUMMARY OF THE INVENTION

The present invention resides in a semiconductor device comprising a gate electrode, a gate insulator film wider than the gate electrode, an active layer, a pair of n- or p-type doped regions formed in the active layer, a pair of silicide layers self-aligned to the gate insulator film, and a selectively grown metallization layer in intimate contact with the silicide layers. The metallization layer is made of a metallic element. The silicide layers each mainly consist of this metallic element and silicon. (Invention 1)

In one embodiment, a top layer of interconnect metal is formed on the gate electrode. This top layer of interconnect metal may be connected with the metallization layer via at least one contact. This structure corresponds to Invention 2. For example, it can be a contact between the top layer of interconnect metal and the source or drain of each TFT (silicide layer). This structure is effective in preventing defective contacts between the quite thin silicide layer described in connection with Figs. 2(A)-2(F) and the top layer of interconnect metal.

The active layer of the TFT needs to be quite thin because of the required characteristics. However, the present invention does not demand that the metallization layer be made quite thin, because the metallization layer in accordance with the present invention is intended to form a silicide layer in the active layer. Rather, the metallization layer may be made sufficiently thick. In the present invention, the whole silicide layer forming the source and drain is in contact with the metallization layer, forming an alloy. The metallization layer is in contact with the top layer of interconnect metal. The concentration of defects of the former is very low. Also, the concentration of defects of the latter is much lower than that of the structure of Figs. 2(A)-2(F), because the metallization layer is sufficiently thick. Accordingly, the total concentration of defects is greatly reduced.

In the fundamental structure described above, the gate interconnect lying in the same layer as the gate electrode may have at least one contact with the metallization layer coupled to the silicide layer. This structure corresponds to Invention 3 and permits the drain 27 (silicide layer 31) shown in Figs. 2(A)-2(F) and the gate interconnect 25 to be

connected without the need to form contact holes.

Generally, the gate layer forming the gate electrode and gate interconnect is isolated from the metallization layer forming the source and drain by an interlayer dielectric. Therefore, contact holes have been always required to make contacts between these two layers. Obviously, the freedom from the contact holes is advantageous to the circuit arrangement.

The metallization layer is used directly as conductive interconnects as mentioned above. Since the resistivity of the metal forming the silicide is higher than that of the interconnect metal by at least one order of magnitude, a layer of another metal having a lower resistivity may be formed on the metallization layer to lower the resistivity of the conductive interconnects. This structure corresponds to Invention 4. The metallization layer may consist chiefly of a material selected from the group consisting of titanium, molybdenum, tungsten, platinum, chromium, and cobalt.

Preferably, the semiconductor device of the construction described above is fabricated by the following process sequence: (1) A gate insulator layer and a gate electrode are formed on an active layer; (2) The gate insulator layer is etched to form a gate insulator film wider than the gate electrode; (3) A metallization layer in intimate contact with the active layer is formed; (4) The active layer is reacted with the metallization layer to form a silicide layer self-aligned to the gate insulator film; and (5) the metallization layer is selectively etched.

The construction of Invention 4 described above may be fabricated by performing a step of forming a layer of a second metal having a resistivity lower than that of the

material of the metallization layer. This layer of the second metal is in intimate contact with the metallization layer. This process step is performed between the steps (3) and (5) above. Where a nonrefractory metal such as aluminum is used, it is better to avoid the execution of the step (4) involving a high temperature. Therefore, this step of forming the second metal layer may be carried out between the processing steps (4) and (5) above.

While the process steps (1)-(5) have been described, fabrication of the source and drain, or doped regions, have not been described in detail. Generally, it is desired to form these doped regions prior to the step (3). In the present invention, the doped regions may or may not be self-aligned to the gate electrode. Where the doped regions are self-aligned to the gate electrode, the following two procedures are conceivable. Most commonly, the step of forming the doped regions is carried out between the steps (1) and (2). This is effective where the sidewalls are used as illustrated in Figs. 2(A)-2(F).

A fabrication step of forming a more heavily doped region may be performed between the steps (2) and (3). This heavily doped region is of the same conductivity type as the doped regions formed by the above-described process steps. Thus, a double-implant lightly doped drain (DI-LDD) structure can be obtained. This step may be carried out after the step (3). In this case, the implants may not be done up to a desired depth, depending on the thickness of the metallization layer. If this step is performed after the step (5), implants can be carried out into other than the double-implant lightly doped drain structure without difficulty.

Where anodization of the gate electrode is utilized, the

formation of the doped region is executed between the processing steps (2) and (3). If the gate interconnect is also exposed during the step (2), the metallization layer forms a junction with the gate interconnect. Therefore, the construction of Invention 3 can be obtained by appropriate selective etching.

After the fundamental steps (1)-(5) described thus far, well-known multi-layer metallization steps may be added. That is, the following three steps are added: (6) An interlayer dielectric is deposited; (7) The interlayer dielectric is etched to form contact holes reaching the metallization layer; and (8) A top layer of interconnect metal in contact with the metallization layer via the contact holes is formed. In this way, the construction of Invention 2 can be derived.

Other objects and features of the invention will appear in the course of the description thereof, which follows.

BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1(A)-1(F) are cross-sectional views illustrating a process sequence for fabricating a semiconductor circuit in accordance with Embodiment 1 of the present invention;

Figs. 2(A)-2(F) are cross-sectional views illustrating the prior art TFT structure;

Figs. 3(A)-3(F) are cross-sectional views illustrating a process sequence for fabricating a semiconductor circuit in accordance with Embodiment 2 of the present invention;

Figs. 4(A)-4(F) are cross-sectional views illustrating a process sequence for fabricating a semiconductor circuit in accordance with Embodiment 3 of the present invention;

Figs. 5(A)-5(F) are cross-sectional views illustrating a process sequence for fabricating a semiconductor circuit in

accordance with Embodiment 4 of the present invention;

Fig. 6 is an enlarged cross section of a TFT in accordance with Embodiment 1, conceptually illustrating the structure of the TFT;

Fig. 7 is an enlarged cross section of a TFT in accordance with Embodiment 3, conceptually illustrating the structure of the TFT;

Figs. 8(A)-8(C) are cross-sectional views illustrating a process sequence for fabricating a semiconductor circuit in accordance with Embodiment 5 of the invention;

Figs. 9(A)-9(E) are cross-sectional views illustrating a process sequence for fabricating a semiconductor circuit in accordance with Embodiment 6 of the invention; and

Fig. 10 is an enlarged cross section of a TFT in accordance with Embodiment 6 of the invention, conceptually illustrating the structure of the TFT.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

EMBODIMENT 1

Figs. 1(A)-1(F) schematically illustrate a process sequence for fabricating TFTs in accordance with the present embodiment. Although these are n-channel TFTs, it is obvious that p-channel TFTs can be manufactured also by forming the source/drain regions out of a p-type semiconductor. The TFTs in accordance with the present embodiment can be disposed at pixels of liquid crystal displays, used in peripheral circuits, in image sensors, and in other integrated circuits.

In the present embodiment, a substrate 1 is made of a glass substrate coated with a silicon oxide film (not shown) having a thickness of 2000 Å. The coating can be made by sputtering or plasma-assisted CVD (PCVD). Then, an

amorphous silicon film is formed to a thickness of 500 Å by PCVD. The method of forming this amorphous silicon film and its film thickness are determined according to the manner in which the present invention is practiced, and no limitations are imposed on them. Also, a crystalline silicon film (e.g., a film of silicon of crystallites or polysilicon) can be exploited.

Then, the amorphous silicon film is crystallized to obtain a crystalline silicon film. Generally, this crystallization is performed by heating at 550-700°C for 1-48 hours. Instead, irradiation of laser light or other intense light may be used. The silicon film crystallized in this way is etched into islands for device isolation, thus defining an active layer region 2. In this active layer region 2, source/drain regions and a channel region will be formed.

Thereafter, a silicon oxide film 3 becoming a gate insulator film is formed to a thickness of 1200 Å. The silicon oxide film 3 is formed by sputtering or PCVD using an organic silane (e.g., TEOS) and oxygen. Then, a polycrystalline phosphorus-doped silicon film becoming gate electrodes is grown to a thickness of 6000-8000 Å (in the present embodiment, 6000 Å). The gate electrodes may be made of a metal silicide and a silicon-metal lamination, as well as silicon.

Subsequently, the polysilicon film is patterned to form gate electrodes 4 and gate interconnects 5. Phosphorus (P) ions that are dopants for imparting the n-type conductivity are implanted into the active layer 2 by an ion implantation method. At this time, the gate electrodes 4 act as a mask, and source/drain regions 6 and 7 are formed in a self-aligned manner (Fig. 1(A)).

Then, annealing making use of laser illumination is done to activate the implanted P ions and to heal the crystallinity of the silicon film deteriorated. This annealing can be lamp annealing employing infrared radiation. In the annealing using infrared radiation (e.g., infrared radiation of 1.2 μm), the infrared radiation is selectively absorbed by the silicon semiconductor. The glass substrate is not heated so much. Furthermore, the heating of the glass substrate can be suppressed by setting the period of each shot of illumination short. In this way, this method is quite useful.

Thereafter, a silicon oxide film is formed to a thickness of 6000 Å to 2 μm (9000 Å, in this embodiment) either by sputtering or by PCVD using TEOS and oxygen. This silicon oxide film is etched by anisotropic dry etching making use of a well-known RIE (reactive ion etching) method. With respect to the sidewalls of the gate electrodes 4 having a height of 9000 Å, the height of silicon oxide is about twice the film thickness of 9000 Å. Therefore, if the etching is made to proceed, almost triangular sidewalls 8 of silicon oxide can be left behind.

In the present embodiment, the width of the triangular sidewalls 8 of the silicon oxide is approximately 3000 Å. This value may be determined, taking account of the thickness of the silicon oxide film, the etching conditions, and the height of the gate electrodes 4. During this process, the gate insulator film is also etched, exposing the source 6 and the drain 7. Furthermore, the top surfaces of the gate electrode 4 and of the gate interconnects 5 are exposed.

The silicon oxide film is left under the gate electrode 4, under the gate interconnects 5, and under their

sidewalls. Since the remaining film is somewhat different from the gate insulator "layer" 3 described above, it is referred to as a gate insulator "film". That is, a gate insulator film 3a is formed under the gate electrode 4 and under its sidewalls. A gate insulator film 3b is obtained under the gate interconnects 5 and under their sidewalls (Fig. 1(B)). Then, a film of Ti (titanium) 9 is formed over the whole surface to a thickness of 3000 to 6000 Å by sputtering (Fig. 1(C)).

The Ti is reacted with the active layer of silicon by thermal annealing to form a silicide. In the present embodiment, the annealing is done at 550 to 600°C to form silicide layer portions 10 and 11 on the source 6 and the drain 7, respectively. It is to be noted that in the present embodiment, silicon is used as the material of the gate interconnects/electrodes. Therefore, the reaction producing the silicide progresses at these portions, which is effective in reducing the resistivities of gate interconnects/electrodes but does not adversely affect other characteristics.

This annealing may be lamp annealing using infrared radiation. Where lamp annealing is utilized, the lamp irradiation is done such that the temperature of the surface of the illuminated surface reaches about 600-1000°C. Where the temperature is 600°C, the lamp irradiation is performed for several minutes. Where the temperature is 1000°C, the lamp irradiation is continued for several seconds. In this embodiment, the thermal annealing is conducted at 450°C after the formation of the Ti film. Depending on the heat resistance of the substrate, the temperature may be above 500°C (Fig. 1(D)).

In the illustrated embodiment, the silicide layer, 10

and 11, is shown to reach the bottom of the active layer. The reaction may be interrupted before the silicide layer arrives at the bottom of the active layer as shown in Fig. 6. No essential difference is produced between these two different methods (Fig. 6).

Then, the Ti film is selectively etched by a well-known photolithography method, using an etchant consisting of a mixture of hydrogen peroxide, ammonia, and water at a ratio of 5:2:2. As a result of the above-described process step, a Ti film (titanium interconnect) 12 connected with the source 6 (silicide 10) via a contact 14a is obtained. Also, a Ti film (titanium interconnect 13) connected with the drain 7 (silicide 11) via a contact 14b is derived. The Ti film 13 is connected with the gate interconnect 5 via a contact 14c (Fig. 1(E)).

Subsequently, an interlayer dielectric 16 is deposited by plasma-assisted CVD (PCVD). Preferably, the dielectric 16 is silicon nitride or silicon oxide. Contact holes 15a and 15b are formed in the dielectric layer. An interconnect metal is deposited by sputtering, and the resulting film is etched to form a top layer of interconnect metal, 17 and 18. Aluminum may be used directly as the interconnect metal, for the following reason. In the present embodiment, the contacts are made of Ti and so the contacts are less deteriorated by the alloying reaction. This is an advantage over the prior art structure illustrated in Figs. 2(A)-2(F) (Fig. 1(F)).

A circuit including the n-channel TFT completed in this way is substantially the same as the circuit constructed as illustrated in Figs. 2(A)-2(F). In the present invention, however, an additional photolithography step is necessary to selectively etch the Ti film. Nonetheless, the number of

the contact holes can be reduced by one in the present embodiment. The interconnect resistance of the present embodiment will make no great difference unless the distance between the drain 7 and the gate interconnect 5 is large.

The present embodiment is further characterized in that the area of the active layer can be reduced. In the structure shown in Figs. 2(A)-2(F), the contacts between the source/drain and the top layer of interconnect metal are formed over the active layer. In contrast, such a limitation is not imposed on the present embodiment. Also, in the structure shown in Figs. 2(A)-2(F), the contact holes are necessary in creating the contacts to the gate interconnect and, therefore, the gate interconnect 25 needs a large area at the contact portion. In the present embodiment, no contact holes are necessary between the Ti film 13 and the gate interconnect 5 and so only a small area suffices. This is advantageous for circuit arrangement.

EMBODIMENT 2

Figs. 3(A)-3(F) schematically illustrate a process sequence for fabricating TFTs in accordance with the present invention. What are fabricated in the present embodiment are n-channel TFTs, but it is obvious that p-channel TFTs can be manufactured by forming the source/drain regions out of a p-type semiconductor. The TFTs in accordance with the present embodiment can be disposed at pixels of liquid crystal displays, used in peripheral circuits, in image sensors, and in other integrated circuits.

In the present embodiment, a substrate 41 is made of a glass substrate coated with a silicon oxide film (not shown) having a thickness of 2000 Å. Islands of a crystalline silicon film (active layer) 42 are formed on the substrate.

A silicon oxide film 43 becoming a gate insulator layer is formed to a thickness of 1200 Å over the crystalline silicon film. Then, a gate electrode 44 and a gate interconnect 45 are formed out of a polycrystalline phosphorus-doped silicon film. Phosphorus ions are implanted as dopants into the active layer 42 to impart the n-type conductivity. During this process step, the gate electrode 44 acts as a mask. Thus, source/drain regions 46 and 47 are formed in a self-aligned manner (Fig. 3(A)).

In the same way as in Embodiment 1, sidewalls 48 are formed on the sidewalls of the gate electrode/interconnect. During this process, the gate insulator layer is also etched, exposing the source 46 and the drain 47. Furthermore, the top surfaces of the gate electrode 44 and of the gate interconnects 45 are exposed. A gate insulator film, 43a and 43b, is formed under the gate electrode 44, under the gate interconnect 45, and under their sidewalls (Fig. 3(B)).

Then, a Ti (titanium) film is formed. In this embodiment, the Ti film, 49, is formed by sputtering over the whole surface to a thickness of 500 to 1000 Å that is thinner than in Embodiment 1 (Fig. 3(C)).

The Ti layer is reacted with the active layer of silicon by thermal annealing to form a silicide layer, 50 and 51, a source 46, and a drain 47 (Fig. 3(D)). Subsequently, an aluminum film 52 having a thickness of 6000-10000 Å is deposited over the whole surface by sputtering (Fig. 3(E)).

Then, the aluminum film and the Ti film are selectively etched. During the etching of the Ti, the previously etched aluminum film is used as a mask. If both aluminum and Ti are processed by wet etching, the aluminum is first etched and then the Ti is etched. Subsequently, the aluminum is

again etched to etch the side surfaces of the aluminum. In consequence, smoother etch steps can be obtained.

As a result of the above-described process steps, a conductive interconnect 53 connected with the source 46 (silicide 50) via a contact 55a is created. Also, a conductive interconnect 54 connected with the drain 47 (silicide 51) via a contact 55b is formed. The interconnect 54 is also connected with a gate interconnect 45 via a contact 55c. In the present embodiment, the interconnect 54 is a Ti-Al multilayer film and has a lower resistivity than that of Embodiment 1. Therefore, if the distance between the drain 47 and the gate interconnect 45 is great, no problem takes place (Fig. 3(F)). A top layer of interconnect metal may be formed by multilayer metallization techniques, in the same way as in Embodiment 1.

EMBODIMENT 3

Figs. 4(A)-4(F) schematically illustrate a process sequence for fabricating TFTs in accordance with the present embodiment. In this embodiment, a substrate 61 is made of a glass substrate coated with a silicon oxide film (not shown) having a thickness of 2000 Å. Islands of a crystalline silicon film (active layer) 62 are formed on the substrate. A silicon oxide film 63 becoming a gate insulator layer is formed to a thickness of 1200 Å over the crystalline silicon film. Then, a gate electrode 64 and a gate interconnect 65 are formed out of a polycrystalline phosphorus-doped silicon film. Phosphorus ions are implanted as dopants into the active layer 62 to impart the n-type conductivity. During this process step, the gate electrode 64 acts as a mask, and doped regions 66 and 67 are formed in a self-aligned manner but with a low dopant concentration of 1×10^{17} to 10^{19} .

atoms/cm³ (Fig. 4(A)).

In the same way as in Embodiment 1, sidewalls 68 are formed on the sidewalls of the gate electrode/interconnect. During this process, the gate insulator layer is also etched, exposing the source 66 and the drain 67. Furthermore, the top surfaces of the gate electrode 64 and of the gate interconnects 65 are exposed. A gate insulator film, 63a and 63b, is formed under the gate electrode 64, under the gate interconnect 65, and under their sidewalls.

Then, phosphorus ions are again implanted as dopants by an ion implantation method to a high dopant concentration of 2×10^{19} to 5×10^{21} atoms/cm³. In this way, a source 69 and a drain 70 are formed (Fig. 4(B)). Then, a film of Ti (titanium) 71 is formed over the whole surface to a thickness of 3000 to 6000 Å by sputtering (Fig. 4(C)).

The Ti layer is reacted with the active layer of silicon by thermal annealing to form a silicide layer, 72 and 73, on a source 69 and on a drain 70 (Fig. 4(D)). Then, the Ti film is selectively etched under the same conditions as in Embodiment 1. As a result of the above-described process steps, a conductive interconnect 74 connected with a source 69 (silicide 72) via a contact 76a is created. Also, a conductive interconnect 75 connected with a drain 70 (silicide 73) via a contact 76b is formed. The interconnect 75 is also connected with a gate interconnect 65 via a contact 76c (Fig. 4(E)).

An interlayer dielectric 78 is deposited by a multilayer metallization technique, in the same manner as in Embodiment 1. Contact holes 77a and 77b are created in this dielectric layer, and conductive interconnects 79 and 80 are formed (Fig. 4(F)).

In the present embodiment, the silicide layer, 72 and

73, may not reach the bottom of the active layer as shown in Fig. 7. A source 69, or a heavily doped region, is left between the lightly doped n-type region 66 and the silicide layer 72 as shown in Fig. 7, which is not seen from Figs. 4(A)-4(F). A similar situation occurs near the drain. This structure is effective in reducing the electric field strength near the source and drain (Fig. 7).

EMBODIMENT 4

Figs. 5(A)-5(F) schematically illustrate a process sequence for fabricating TFTs in accordance with the present embodiment. In this embodiment, a substrate 81 is made of a glass substrate coated with a silicon oxide film (not shown) having a thickness of 2000 Å. Islands of a crystalline silicon film (active layer) 82 are formed on the substrate. A silicon oxide film 83 becoming a gate insulator layer is formed to a thickness of 1200 Å over the crystalline silicon film. Then, gate electrodes 84 and 85 are formed from an aluminum film (Fig. 5(A)).

Subsequently, the gate electrodes and the gate insulator layer are processed, using the anodization techniques disclosed in the above-cited Japanese Patent Unexamined Publication Nos. 169974/1995, 169975/1995, and 218932/1995, thus producing the illustrated structure. The gate electrodes are coated with a barrier-type anodic oxide. In this manner, gate electrodes 84a, 85a and a gate insulator film, 83a and 83b, are obtained (Fig. 5(B)).

Then, phosphorus ions are implanted as dopants into the active layer 82 to impart the n-type conductivity. During this process step, the gate electrodes 84a and 85a serve as a mask, and doped regions 86, 87, and 88 are formed in a self-aligned manner (Fig. 5(C)).

Then, a film of Ti (titanium) 89 is formed over the

whole surface to a thickness of 3000 to 6000 Å by sputtering. The Ti layer is reacted with the active layer of silicon by thermal annealing to form a silicide layer, 90-92, in the doped regions 86-88 (Fig. 5(D)).

Thereafter, the Ti film is selectively etched under the same conditions as in Embodiment 1. As a result of the above-described process steps, conductive interconnects 93 and 94 are produced (Fig. 5(E)). Then, an interlayer dielectric 95 is deposited by a multilayer metallization technique, in the same manner as in Embodiment 1. Contact holes are created in this dielectric, and conductive interconnects 96 and 97 are formed (Fig. 5(F)).

EMBODIMENT 5

Figs. 8(A)-8(C) schematically illustrate a process sequence for fabricating TFTs in accordance with the present embodiment. In this embodiment, a substrate 101 is made of a glass substrate coated with a silicon oxide film (not shown) having a thickness of 2000 Å. Islands of a crystalline silicon film (active layer) 102 having a source 106 and a drain 107, a gate insulator film 103a, and a gate electrode 104 are formed on the substrate, using the technique described in Embodiment 4. At the same time, gate interconnects 105 having a gate insulator film 103b are formed (Fig. 8(A)).

Then, a film of Ti (titanium) 109 is formed over the whole surface to a thickness of 3000 to 6000 Å by sputtering. The Ti layer is reacted with the active layer of silicon by thermal annealing to form a silicide layer, 110-111, in the source 106 and in the drain 107 (Fig. 8(B)).

Thereafter, the Ti film is selectively etched under the same conditions as in Embodiment 1. As a result of the

above-described process steps, a conductive interconnect 112 connected with the source 106 (silicide 110) via a contact 114a is obtained. Also, a conductive interconnect 113 connected with the drain 107 (silicide 111) via a contact 114b is produced. The interconnect 113 overlaps the gate interconnect 105 but no junction is formed because the gate interconnect 105 is coated with a barrier-type, highly insulating anodic oxide. However, this portion 115 is effectively used as a capacitance. This capacitance is used as an auxiliary capacitance in an active matrix liquid crystal display (Fig. 8(C)).

EMBODIMENT 6

Figs. 9(A)-9(E) schematically illustrate a process sequence for fabricating TFTs in accordance with the present embodiment. In this embodiment, a substrate 121 is made of a glass substrate coated with a silicon oxide film (not shown) having a thickness of 2000 Å. Islands of a crystalline silicon film (active layer) 122 are formed on the substrate. A silicon oxide film 123 becoming a gate insulator layer is formed to a thickness of 1200 Å over the crystalline silicon film. Then, gate electrodes 124 and 125 are formed out of an aluminum film. Phosphorus ions are implanted as dopants into the active layer 122 to impart the n-type conductivity. During this process step, the gate electrodes 124 and 125 act as a mask, and doped regions 126, 127, and 128 are formed in a self-aligned manner but with a low dopant concentration of 1×10^{17} to 10^{19} atoms/cm³ (Fig. 9(A)).

Then, the gate insulator layer 123 is etched by a well-known photolithography method to expose the doped regions 126-128 partially as shown. In this manner, a gate

insulator film, 123a and 123b, is obtained.

Then, a film of Ti (titanium) 129 is formed over the whole surface to a thickness of 3000 to 6000 Å by sputtering (Fig. 9(B)).

The Ti layer is reacted with the active layer of silicon by thermal annealing to form a silicide layer, 130-132, in the doped regions 126-128. Thereafter, the Ti film is selectively etched to form conductive interconnects 133 and 134 (Fig. 9(C)). Subsequently, those portions of the gate insulator film, 123a and 123b, which overlap the lightly doped region 127 are etched (Fig. 9(D)).

Then, phosphorus ions are again implanted as dopants by an ion implantation method to a high dopant concentration of 2×10^{19} to 5×10^{21} atoms/cm³. In this way, a heavily doped region 135 is formed (Fig. 9(E)).

The present embodiment is characterized in that the resistivity of the central doped region is reduced by the heavy doping, thus decreasing the series resistance. Although not seen from Figs. 9(A)-9(E), a heavily doped region 136 is left between the silicide layer, 130 and 132, at both ends of the TFT and each lightly doped region, 126, 128, as shown in the enlarged view of Fig. 10. This structure is effective in reducing the electric field strength near the source and drain (Fig. 10).

In the present invention, a silicide layer is formed from a metallization layer in the source and drain in a self-aligned manner. This metallization layer is used for conductive interconnects or a contact pad to thereby reduce the circuit resistivity. Also, the circuit density can be enhanced. Especially, the present invention yields the following advantages: (1) No mask alignment problems take place; and (2) No problems occur in forming contacts. In

this way, the invention can improve the characteristics of TFTs and semiconductor circuits, production yield, reliability, and productivity.

WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

- a gate electrode;
- a gate insulator film wider than said gate electrode;
- an active layer;
- a pair of n- or p-type doped regions formed in said active layer;
- a pair of silicide layers self-aligned to said gate insulator film, said silicide layers consisting mainly of a metal material and silicon;
- a first metallization layer in intimate contact with said silicide layers, said first metallization layer being made of said metal material; and
- a top layer of interconnect metal formed over said gate electrode and connected with said first metallization layer via at least one contact.

2. A device according to claim 1, wherein conductive interconnects and said gate electrode are formed in a common layer, and wherein said conductive interconnects are connected with said first metallization layer via at least one contact.

3. A device according to claim 1, further comprising a second metallization layer that is in intimate contact with said first metallization layer, similar in geometry to said first metallization layer, and made of a material having a smaller resistivity than the material of said first metallization layer.

4. A device according to claim 1, wherein said first

metallization layer consists mainly of an element selected from the group consisting of titanium, molybdenum, tungsten, platinum, chromium, and cobalt.

5. A semiconductor device comprising:

- a gate electrode formed in a layer;

- a gate insulator film wider than said gate electrode;

- an active layer;

- a pair of n- or p-type doped regions formed in said active layer;

- a pair of silicide layers self-aligned to said gate insulator film, said silicide layers consisting mainly of a metal material and silicon;

- a first metallization layer in intimate contact with said silicide layers, said first metallization layer being made of said metal material;

- a second metallization layer that is in intimate contact with said first metallization layer, similar in geometry to said first metallization layer, and made of a material having a smaller resistivity than the material of said first metallization layer; and

- conductive interconnects formed in the same layer as said gate electrode and connected with said first metallization layer via at least one contact.

6. A device according to claim 5, wherein said first metallization layer consists mainly of an element selected from the group consisting of titanium, molybdenum, tungsten, platinum, chromium, and cobalt.

7. A method of fabricating a semiconductor device,

comprising the steps of:

forming a gate insulator layer and a gate electrode on an active layer;

etching said gate insulator layer to form a gate insulator film wider than said gate electrode;

forming a first metallization layer out of a material in intimate contact with said active layer;

reacting said active layer with said first metallization layer to form silicide layers self-aligned to said gate insulator film; and

selectively etching said first metallization layer.

8. A method according to claim 7, wherein a step of forming a second metallization layer out of a material having a resistivity smaller than that of the material of said first metallization layer is performed between said step of reacting said active layer with said first metallization layer and said step of selectively etching said first metallization layer such that said second metallization layer is in intimate contact with said first metallization layer.

9. A method according to claim 7, wherein a step of forming an n- or p-type doped region in a self-aligned manner in the active region, using said gate electrode, is performed between said step of forming said gate insulator layer and said gate electrode on the active layer and said step of etching said gate insulator layer.

10. A method according to claim 9, wherein a step of forming a more heavily doped region than said n- or p-type doped region is performed between said step of etching said gate

insulator layer and said step of forming said first metallization layer such that said more heavily doped region is of the same conductivity type as said n- or p-type doped region.

11. A method according to claim 7, wherein a step of forming an n- or p-type doped region in said active region in a self-aligned manner, using said gate electrode or both said gate electrode and said gate insulator film, is performed between said step of etching said gate insulator layer and said step of forming said first metallization layer.

12. A method according to claim 7, wherein after said step of selectively etching said first metallization layer, an interlayer dielectric is deposited, said interlayer dielectric is etched to form contact holes reaching said first metallization layer, and a top layer of interconnect metal connected with said first metallization layer via said contact holes is formed.

ABSTRACT OF THE DISCLOSURE

There is disclosed a method of fabricating TFTs having reduced interconnect resistance by having improved contacts to source/drain regions. A silicide layer is formed in intimate contact with the source/drain regions. The remaining metallization layer is selectively etched to form a contact pad or conductive interconnects.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Declaration and Power of Attorney For Patent Application

特許出願宣言書及び委任状

Japanese Language Declaration

日本語宣言書

下記の氏名の発明者として、私は以下の通り宣言します。

As a below named inventor, I hereby declare that:

私の住所、私書箱、国籍は下記の私の氏名の後に記載された通りです。

My residence, post office address and citizenship are as stated next to my name.

下記の名称の発明に関して請求範囲に記載され、特許出願している発明内容について、私が最初かつ唯一の発明者（下記の氏名が一つの場合）もしくは最初かつ共同発明者であると（下記の名称が複数の場合）信じています。

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

SEMICONDUCTOR DEVICE AND

METHOD OF FABRICATING THE SAME

上記発明の明細書（下記の欄でx印がついていない場合は、本書に添付）は、

the specification of which is attached hereto unless the following box is checked:

☐ 月 日に提出され、米国出願番号または特許協定条約
 国際出願番号を _____ とし、
 （該当する場合） _____ に訂正されました。

☐ was filed on _____
 as United States Application Number or
 PCT International Application Number
 _____ and was amended on
 _____ (if applicable).

私は、特許請求範囲を含む上記訂正後の明細書を検討し、内容を理解していることをここに表明します。

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

私は、連邦規則法典第37編第1条56項に定義されるとおり、特許資格の有無について重要な情報を開示する義務があることを認めます。

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Japanese Language Declaration (日本語宣言書)

私は、米国法典第35編119条(a)-(d)項又は365条(b)項に基づき下記の、米国以外の国の少なくとも一カ国を指定している特許協力条約365(a)項に基づく国際出願、又は外国での特許出願もしくは発明者証の出願についての外国優先権をここに主張するとともに、優先権を主張している、本出願の前に出願された特許または発明者証の外国出願を以下に、枠内をマークすることで、示しています。

Prior Foreign Application(s)

外国での先行出願

8-307443

(Number)
(番号)

Japan

(Country)
(国名)

(Number)
(番号)

(Country)
(国名)

私は、第35編米国法典119条(e)項に基づいて下記の米国外特許出願規定に記載された権利をここに主張いたします。

(Application No.)
(出願番号)

(Filing Date)
(出願日)

私は、下記の米国法典第35編120条に基づいて下記の米国外特許出願に記載された権利、又は米国を指定している特許協力条約365条(c)に基づき権利をここに主張します。また、本出願の各請求範囲の内容が米国法典第35編112条第1項又は特許協力条約で規定された方法で先行する米国外特許出願に開示されていない限り、その先行米国外出願書提出日以降で本出願書の日本国内または特許協力条約国際提出日までの期間中に入手された、連邦規則法典第37編1条56項で定義された特許資格の有無に関する重要な情報について開示義務があることを認識しています。

(Application No.)
(出願番号)

(Filing Date)
(出願日)

(Application No.)
(出願番号)

(Filing Date)
(出願日)

私は、私自身の知識に基づいて本宣言書中で私が行なう表明が真実であり、かつ私の入手した情報と私の信じることに基づく表明が全て真実であると信じていること、さらに故意になされた虚偽の表明及びそれと同等の行為は米国法典第18編第1001条に基づき、罰金または拘禁、もしくはその両方により処罰されること、そしてそのような故意による虚偽の声明を行なえば、出願した、又は既に許可された特許の有効性が失われることを認識し、よってここに上記のごとく宣誓を致します。

I hereby claim foreign priority under Title 35, United States Code, Section 119 (a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Priority Not Claimed

優先権主張なし

October 31, 1996

(Day/Month/Year Filed)
(出願年月日)

(Day/Month/Year Filed)
(出願年月日)

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below.

(Application No.)
(出願番号)

(Filing Date)
(出願日)

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s), or 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code Section 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of application.

(Status: Patented, Pending, Abandoned)
(現況: 特許許可済、係属中、放棄済)

(Status: Patented, Pending, Abandoned)
(現況: 特許許可済、係属中、放棄済)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Japanese Language Declaration
(日本語宣言書)

委任状 私は下記の発明者として、不出願に関する一切の手続きを米特許審判局に対して遂行する弁理士または代理人として、下記の者を指名いたします。(弁理士、または代理人の氏名及び登録番号を明記のこと)

Scott C. Harris Reg. No. 32,030

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith (list name and registration number)

書類送付先

Scott C. Harris
FISH & RICHARDSON
4225 Executive Square, Ste. 1400
La Jolla, CA 92037

Send Correspondence to:

直接電話連絡先 (名前及び電話番号)

Scott C. Harris
FISH & RICHARDSON
4225 Executive Square, Ste. 1400
La Jolla, CA 93027

Direct Telephone Calls to: (name and telephone number)

唯一または第一発明者名	Full name of sole or first inventor	
	Hisashi OHTANI	
発明者の署名	日付	
	Inventor's signature	Date
	Hisashi Ohtani	October 21, 1997
住所	Residence	
	Kanagawa, Japan	
国籍	Citizenship	
	Japanese	
私書箱	Post Office Address	
	c/o SEMICONDUCTOR ENERGY LABORATORY CO., LTD.	
	398, Hase, Atsugi-shi, Kanagawa-ken 243 Japan	
第二共同発明者	Full name of second joint inventor, if any	
	Etsuko FUJIMOTO	
第二共同発明者	日付	
	Second inventor's signature	Date
	Etsuko Fujimoto	October 21, 1997
住所	Residence	
	Kanagawa, Japan	
国籍	Citizenship	
	Japanese	
私書箱	Post Office Address	
	c/o SEMICONDUCTOR ENERGY LABORATORY CO., LTD.	
	398, Hase, Atsugi-shi, Kanagawa-ken 243 Japan	

(第三以降の共同発明者についても同様に記載し、署名をすること)

(Supply similar information and signature for third and subsequent joint inventors.)

SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE SAME

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a TFT structure or a semiconductor integrated circuit construction having TFTs and to a method of fabricating such a structure. Especially, the invention relates to conductive interconnects for TFTs or for a semiconductor integrated circuit having TFTs. Also, the invention relates to a method of forming such interconnects.

2. Description of the Related Art

Techniques for using TFTs (thin-film transistors) in an integrated circuit such as an active matrix liquid crystal display or image sensor fabricated on a glass substrate have been well known. Making reliable contacts of the semiconductor regions (such as source and drain) of the TFTs with conductive interconnects is important for such an integrated circuit. Also, decreasing the resistivity of the circuit is important. These requirements become more important and technical difficulties arise as the circuit device density increases.

The former requirement is associated with the fact that the used semiconductor thin film is quite thin. Generally, a semiconductor thin film is required to have good characteristics. However, it is quite difficult to form contacts on a semiconductor thin film as thin as hundreds of Angstroms. During fabrication of contact holes, overetching is highly likely to occur, forming holes or pits in the semiconductor holes. This phenomenon takes place, because the etch rates of silicon oxide and silicon nitride generally used as interlayer dielectrics and the etch rate

of silicon (especially, in the case of dry etching) used as a semiconductor thin film are not very high.

With respect to the latter requirement, many resistors are made of thin films of semiconductors. Decreasing the semiconductor thin film portions of the circuit is a fruitful countermeasure. However, the problem cannot be solved simply by devising the circuit arrangement because of design rule problems.

A method for solving the latter problem has been proposed. This method consists of siliciding almost all portions corresponding to the source and drain of each TFT. An example of this proposed method is next described by referring to Figs. 2(A)-2(F).

A semiconductor film, or an active layer, 22 is formed on a substrate 21. A gate insulator layer 23 is formed over this semiconductor film 22. Then, a gate electrode 24 and a gate interconnect 25 are formed on the insulator layer. The gate electrode 24 and the gate interconnect 25 are in the same layer. That is, they are fabricated at the same time. Doped regions such as a source 26 and a drain 27 are formed in the active layer 22 (Fig. 2(A)).

Thereafter, a sidewall dielectric 28 is deposited on the sidewalls of the gate electrode 24 and of the gate interconnect 25 by a well-known anisotropic etching technique. This is normally accomplished by coating the whole surface with an insulator and then performing anisotropic etching. At this time, the gate insulator layer 23 is also etched, exposing the surface of the active layer. A gate insulator film island 23a is formed under the gate electrode 24. Also, a gate insulator film island 23b is formed under the gate interconnect 25 (Fig. 2(B)).

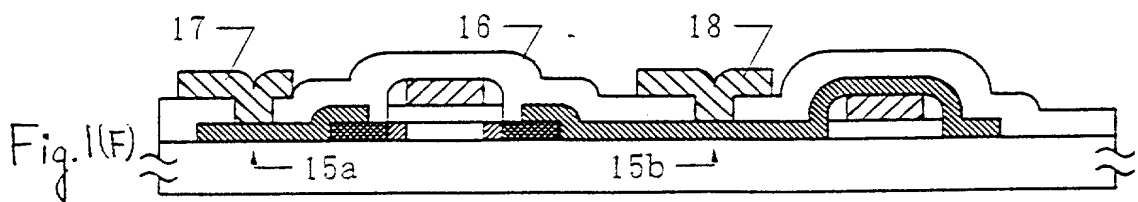
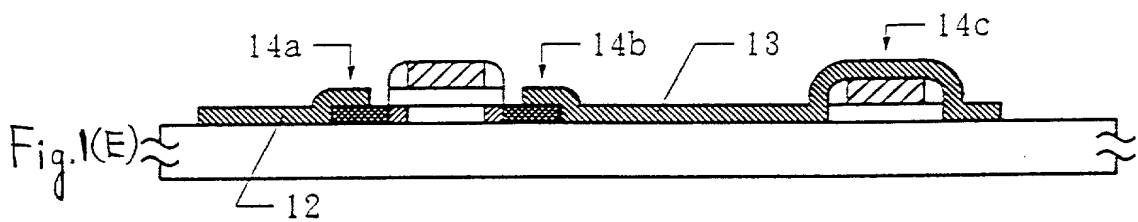
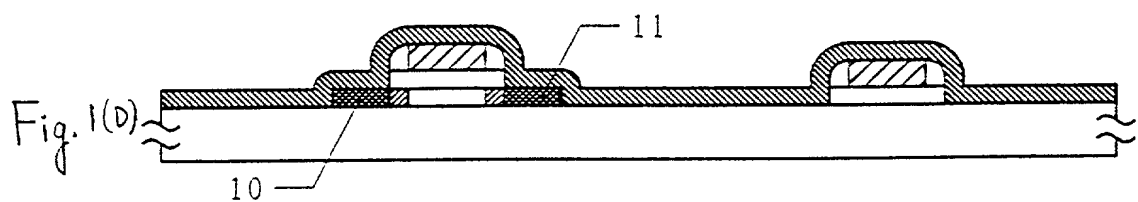
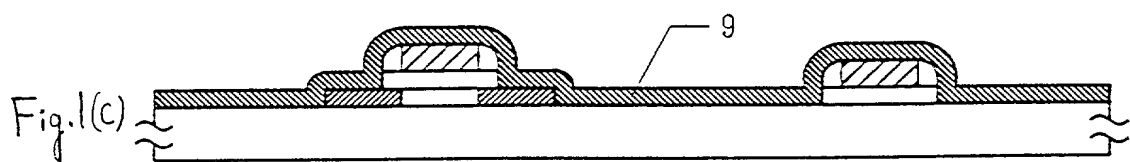
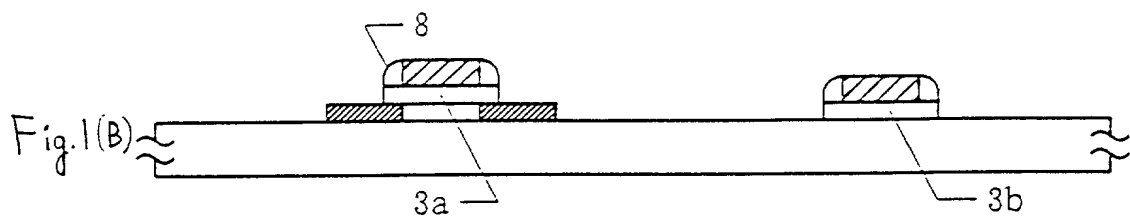
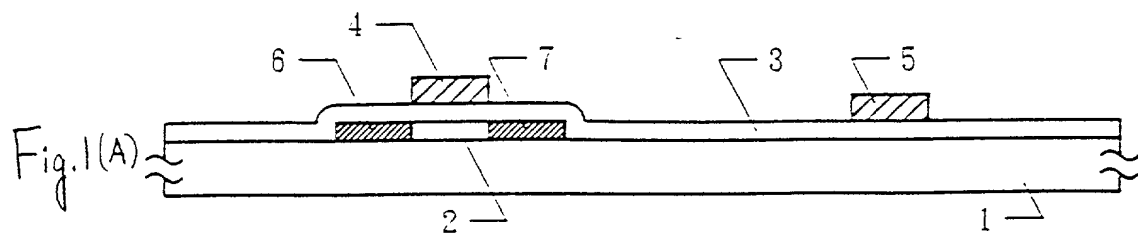
Then, a metallization layer 29 is deposited over the

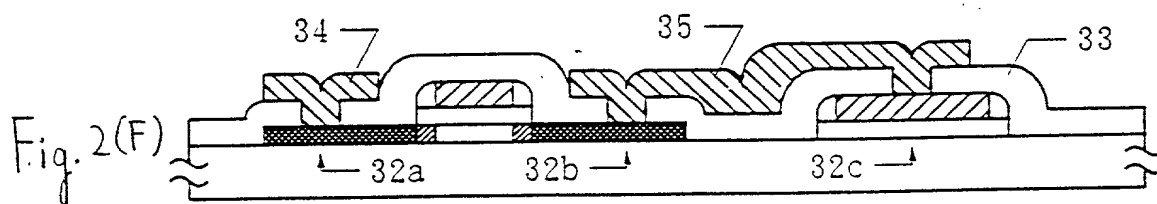
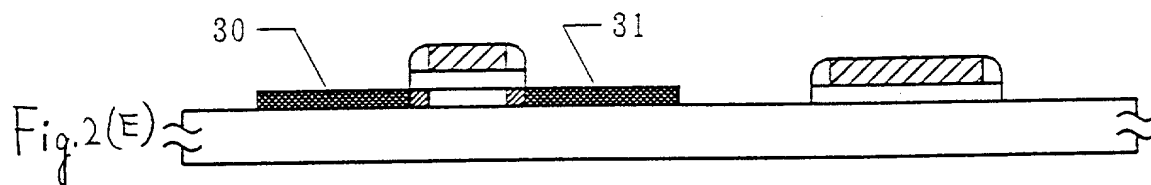
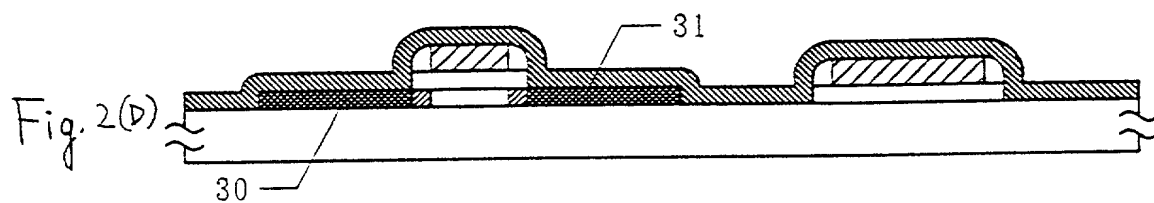
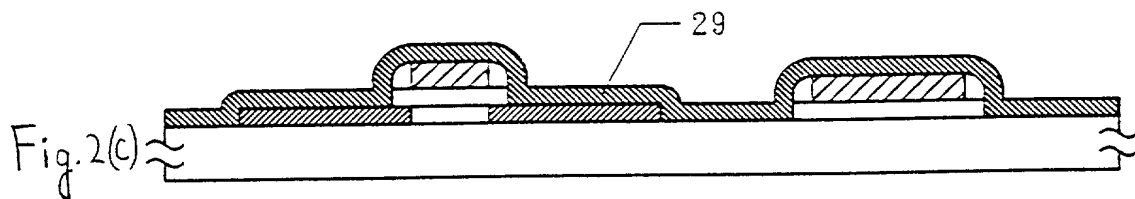
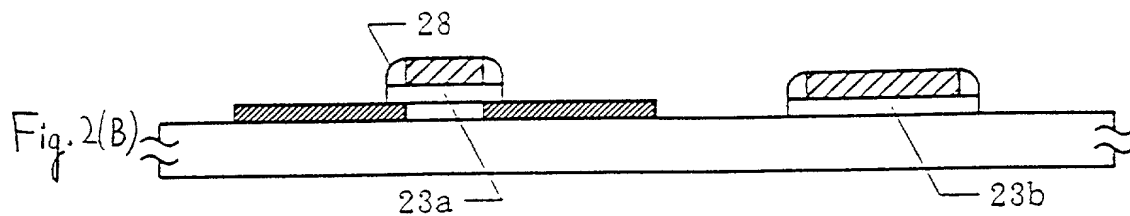
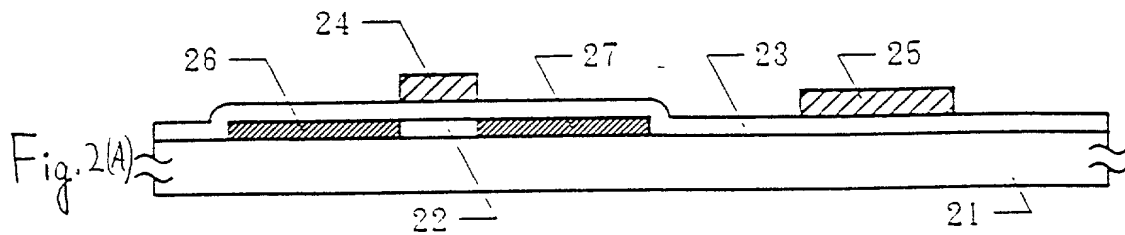
whole surface (Fig. 2(C)). The metallization layer 29 and the active layer 22 are made to react with each other at their interface by thermal annealing, rapid thermal annealing, photo-annealing, or other means, thus obtaining a silicide layer, 30 and 31. The reaction may be made to progress to such an extent that the silicide layer reaches the bottom of the active layer as shown. Alternatively, the reaction may be stopped before the silicide layer reaches the bottom. In either case, the reaction starts from the interface between the metallization layer 29 and the active layer 22 and so the source and drain under the sidewall 28 remain semiconductive in nature (Fig. 2(D)).

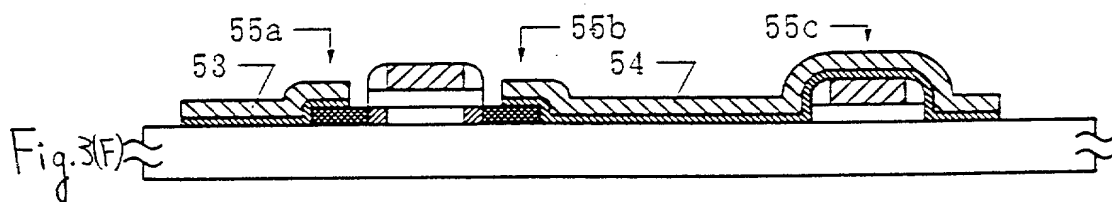
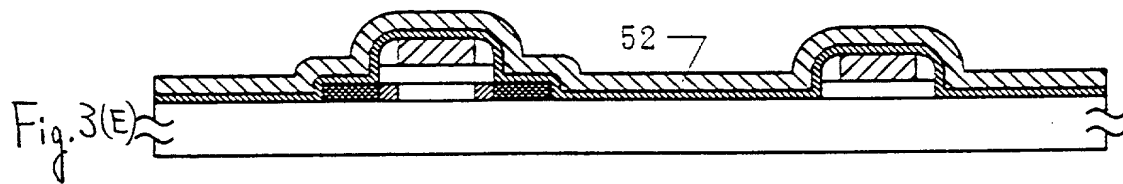
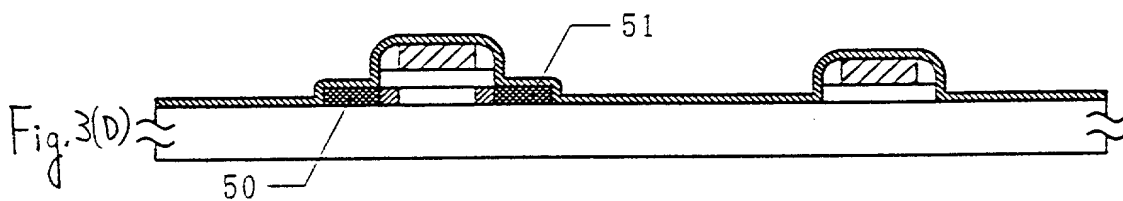
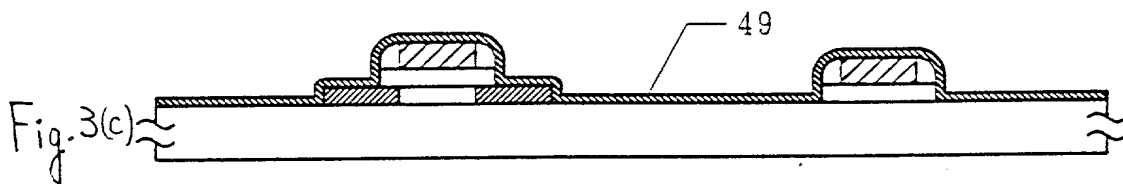
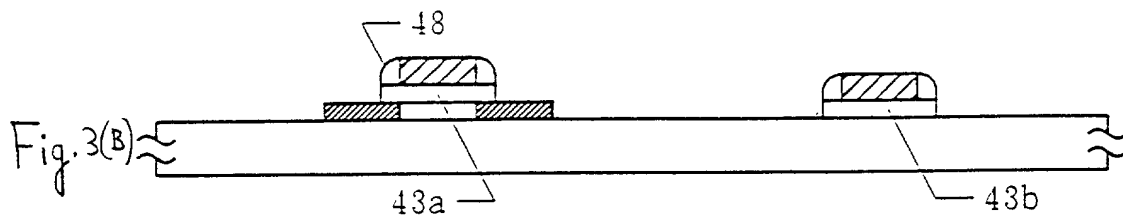
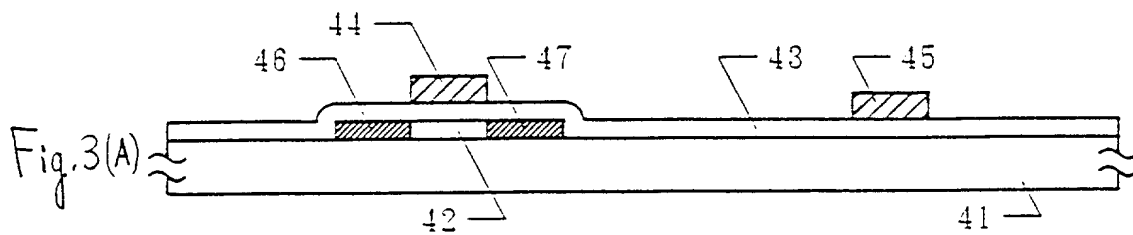
Subsequently, the unreacted metallization layer portions are fully removed (Fig. 2(E)). Finally, a top layer of interconnect metal, 34 and 35, is formed on the interlayer dielectric 33 by a well-known, multi-level metallization technique. The top layer of interconnect metal forms contacts, 32a and 32b together with the silicide layer, 30 and 31. Also, the top layer of interconnect metal forms a contact 32c together with the gate interconnect 25.

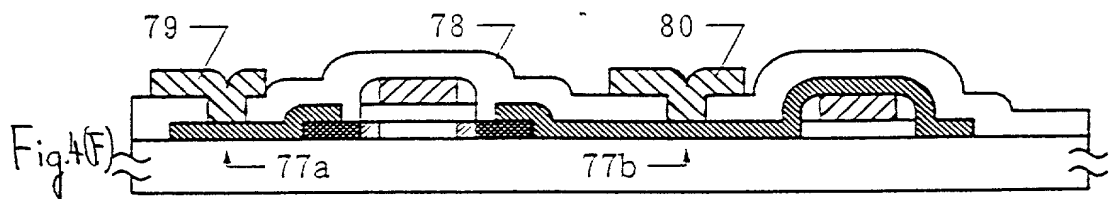
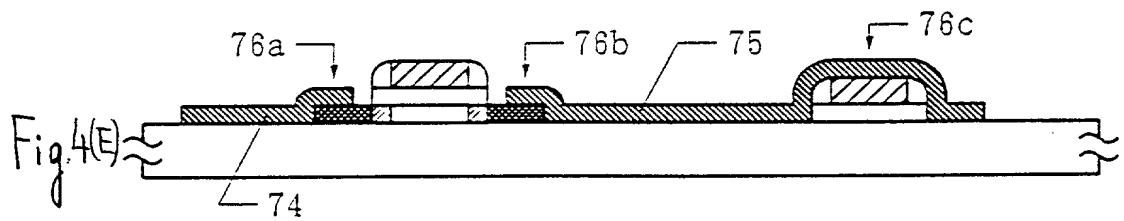
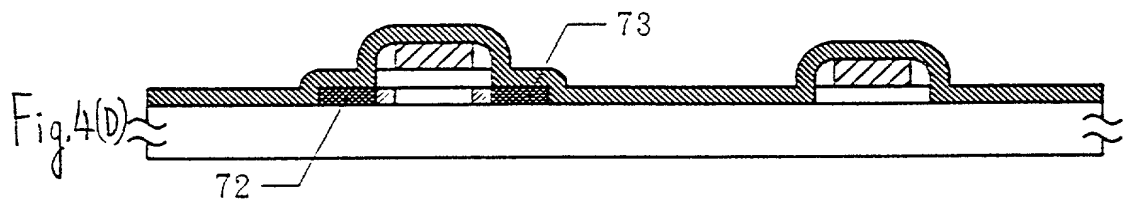
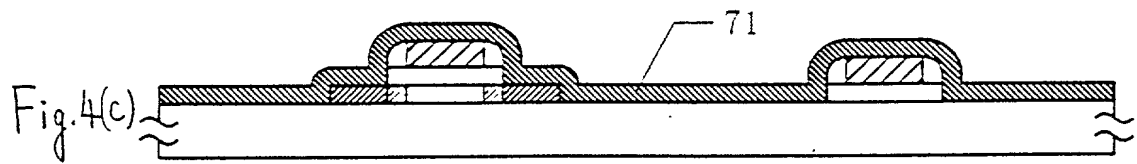
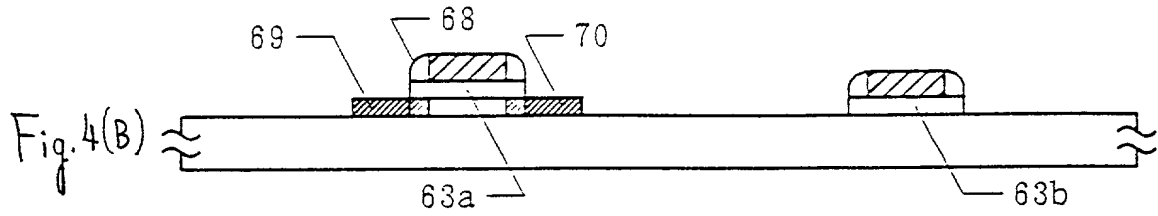
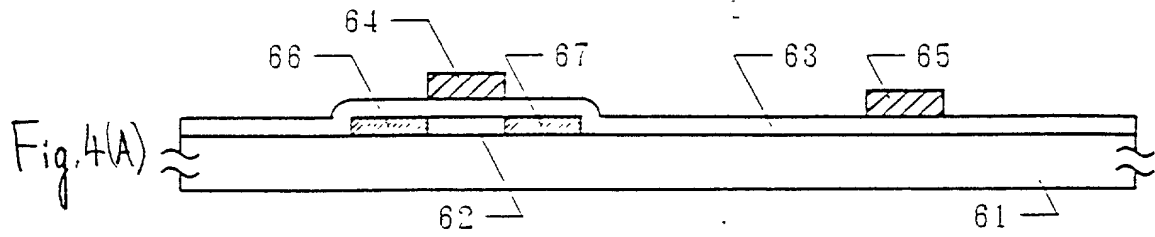
In the example already described in conjunction with Figs. 2(A)-2(E), anisotropically etched sidewalls are used. Techniques for anodizing gate electrodes, as disclosed in Japanese Patent Unexamined Publication Nos. 169974/1995, 169975/1995, and 218932/1995 may also be employed.

With this method, the resistivity of the circuit portions including TFTs can be reduced, because silicides have lower resistivities than semiconductor materials. However, the problems produced where contact holes are created can be hardly solved, because the etch rates of silicides and silicon oxide or silicon nitride are not sufficiently high where a dry etching method is used. It is









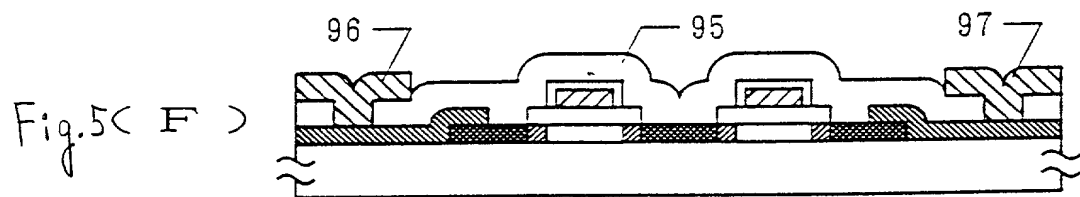
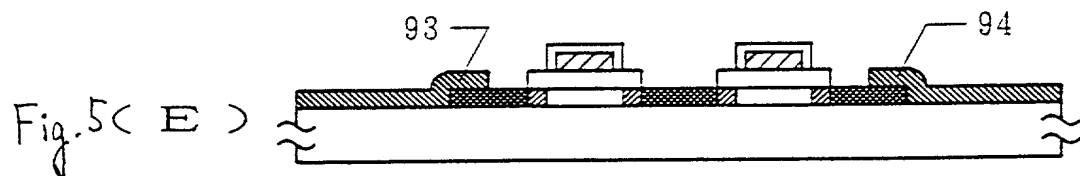
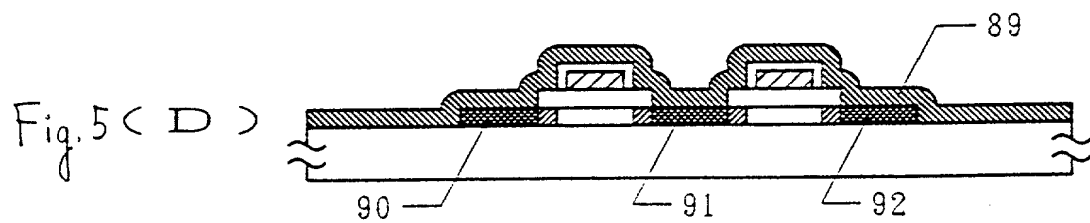
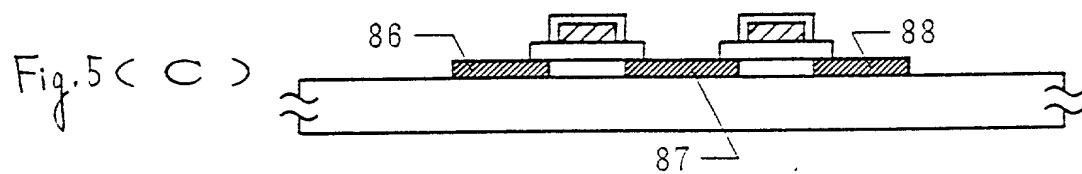
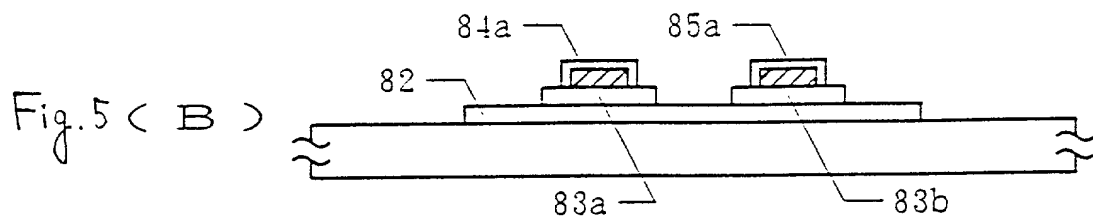
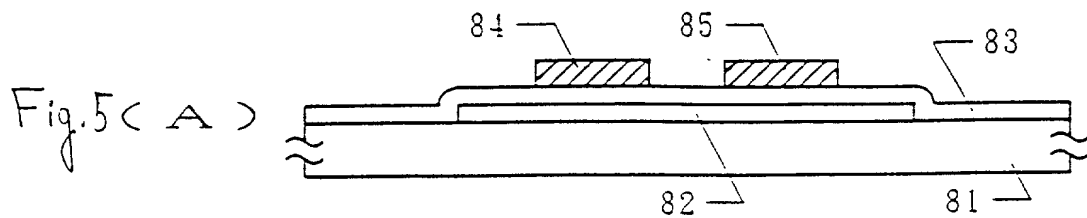


Fig. 6

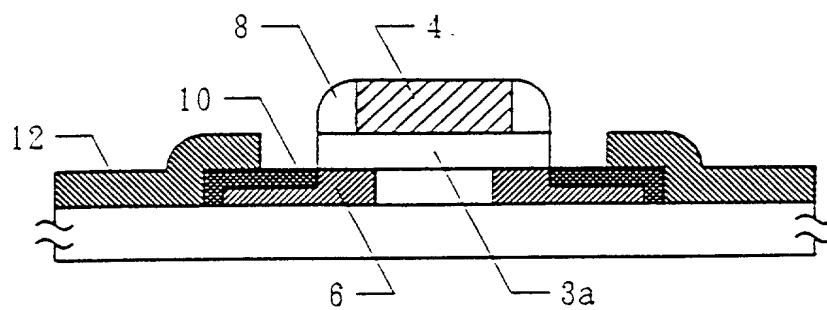


Fig. 7

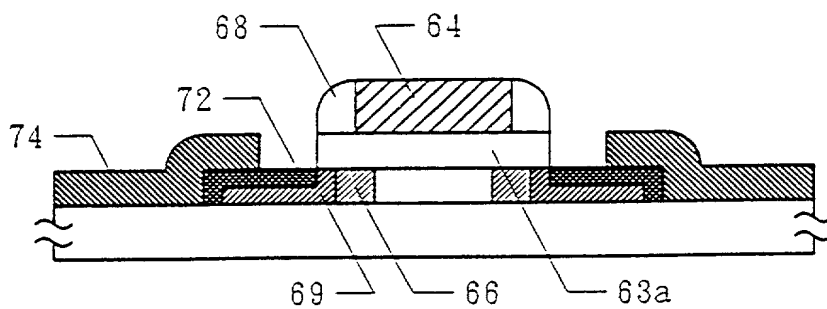


Fig. 8 (A)

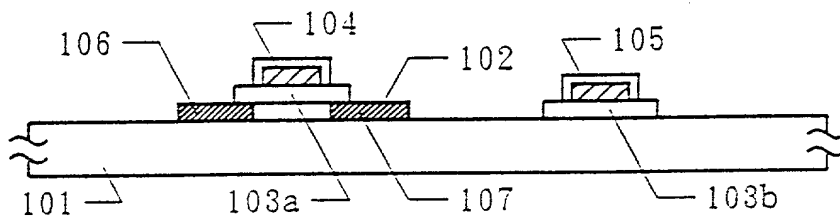


Fig. 8 (B)

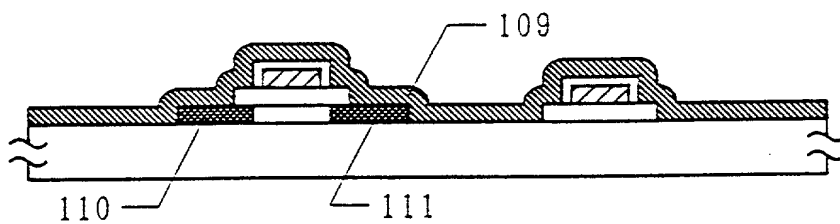


Fig. 8 (C)

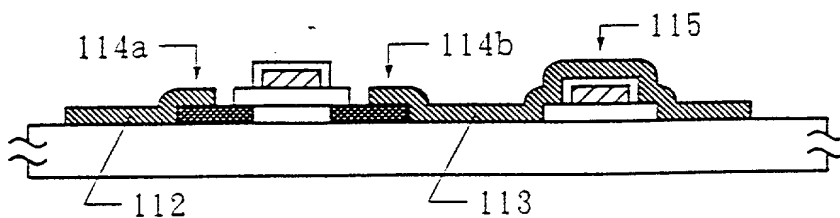


Fig. 9 (A)

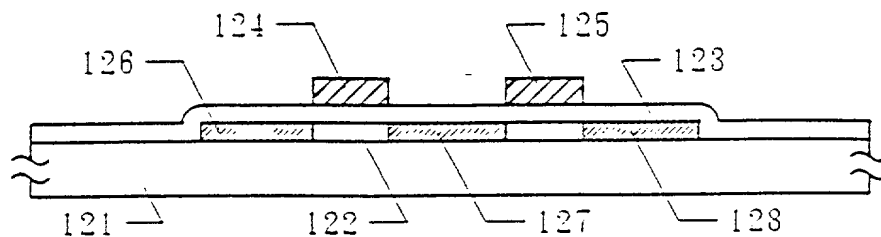


Fig. 9 (B)

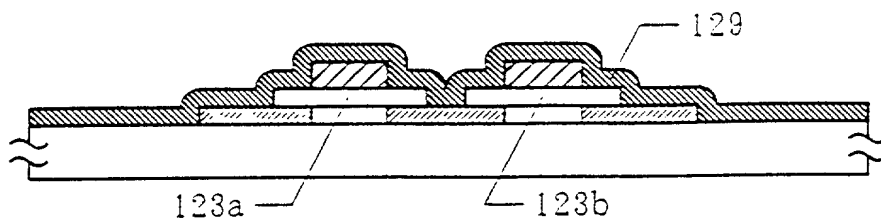


Fig. 9 (C)

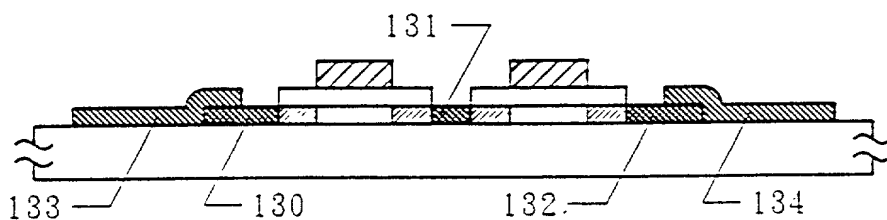


Fig. 9 (D)

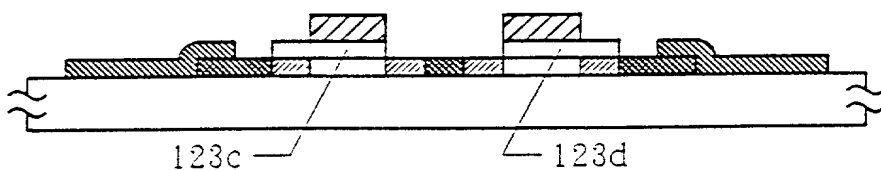


Fig. 9 (E)

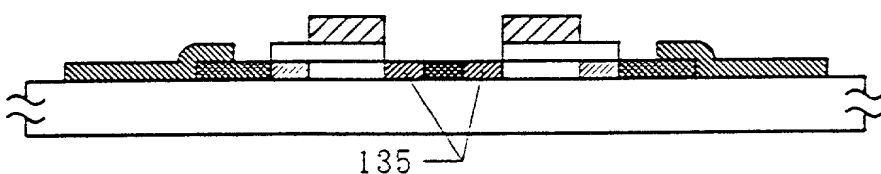


Fig. 10

